REMARKS

This is intended as a full and complete response to the Final Office Action dated July 12, 2005, having a shortened statutory period for response set to expire on October 12, 2005. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 11 and 14-24 are pending in the application. Claims 11 and 14-24 remain pending following entry of this response. Claims 11 and 19 have been amended to more clearly recite features previously presented. Applicants submit that the amendments do not introduce new matter and do not raise new issues.

Claim Rejections - 35 U.S.C. § 102

Claims 11-15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by *Lu* (6,218,693). Applicants respectfully traverse this rejection.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

In this case, *Lu* does not disclose "each and every element as set forth in the claim". For example, *Lu* does not disclose a doped region formed completely within the source/drain electrode to contact the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed substantially underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. The Examiner argues that *Lu* discloses a memory cell having a doped region as claimed in Col. 2, lines 12-14. However, the passages and Figures cited by the

Examiner are in fact directed to a doped conductive layer (reference numeral 19 (N+)) projecting from the source-drain-diffusion region (reference numeral 17 (N-)). As disclosed in *Lu*, the doped conductive layer 19 is not formed completely within the source-drain-diffusion region 17. Instead, the doped conductive layer 19 is formed adjacent the source-drain-diffusion region 17. Furthermore, the doped conductive layer 19 projects underneath the insulating layer (reference numeral 20) adjoining the bit line contact (reference numeral 30') such that a substantial portion of the doped conductive layer is positioned below the insulating layer 20 surrounding the bit line contact. *See* Figures 1, 2 and 12 of *Lu*. In contrast, the doped region as claimed is formed substantially underneath the bit line contact and does not extend significantly underneath the surrounding insulating layer. Claims 11 and 19 have been amended to more clearly recite these features which have been previously presented. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Lu* as applied to claims 11-15, 17 and 18 above, and further in view of *Dennison et al.* (6,429,069, hereinafter *Dennison*).

Applicants respectfully traverse this rejection. The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143. The present rejection fails to establish at least the third criteria.

As discussed above, *Lu* does not disclose "each and every element as set forth in the claim". *Dennison* discloses a method for fabricating a memory cell utilizing self-aligned contact openings. The references cited by the Examiner, either alone or in

combination, fail to teach, show or suggest a doped region formed completely within the source/drain electrode to contact the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed substantially underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Lu* as applied to claims 11-15, 17 and 18 above, and further in view of *Bollinger et al.* (6,762,136, hereinafter *Bollinger*).

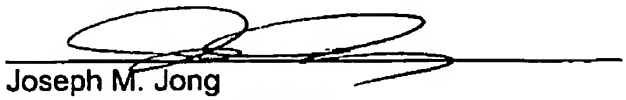
Applicants respectfully traverse this rejection. The present rejection fails to establish that the prior art reference (or references when combined) teach or suggest all the claim limitations. As discussed above, *Lu* does not disclose "each and every element as set forth in the claim". *Bollinger* discloses a rapid thermal processing of substrates. The references cited by the Examiner, either alone or in combination, fail to teach, show or suggest a doped region formed completely within the source/drain electrode between the substrate and the filling of the bit-line contact, wherein the doped region comprises a locally limited electrically conductive contact layer which is formed substantially underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. Therefore, the claims are believed to be allowable, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted,



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